REMARKS

Claims 3-22 are all the claims presently pending in the application. Claims 3, 6, 8, 14 and 17 have been amended to more particularly define the invention. Claims 18-22 have been added to claim additional features of the claimed invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 3-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata, et al. (U.S. Patent No. 5,880,500).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as claimed in claim 3) is directed to a method for manufacturing a semiconductor device (e.g., an n-type metal oxide semiconductor field effect transistor (NMOSFET)).

The method includes implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse short channel effect to form arsenic ion implanted regions, implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted regions, and performing a heat treatment to activate the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions which include phosphorous ions and extend beyond the source/drain regions. Importantly, the first acceleration energy is no greater than 15keV.

Conventional methods of forming source/drain regions in a semiconductor device (e.g., an NMOSFET) include implanting arsenic at a high acceleration energy of about 50 keV in the source/drain region. However, as channel length and source/drain regions have become smaller, a reverse short channel effect has been realized in which the threshold

voltage fluctuates largely for with a change in the length of the gate. The acceleration energy of implantation could be lowered to eliminate this reverse short channel effect, but this would result in an undesirable increase in p-n junction leakage current.

The claimed method, on the other hand, implants arsenic at a first acceleration energy which is no greater than 15keV (e.g., to form the source and drain regions). The inventors found that implanting phosphorous into the arsenic implanted regions of the substrate helps to inhibit a leakage current. Thus, the claimed invention is able to implant arsenic at an acceleration energy (e.g., a low acceleration energy) which inhibits a reverse short channel effect without increasing the p-n junction leakage current (Application at page 14, lines 13-22).

II. THE IWATA REFERENCE

The Examiner alleges that Iwata makes obvious the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Iwata.

Iwata discloses a method of forming a semiconductor device in which phosphorous is implanted in a silicon substrate to form a first impurity diffusion region, and arsenic is later implanted to form a second impurity diffusion region (Iwata at Figure 1; col. 10, line 57-col. 11, line 15). Specifically, Iwata discloses a method in which first impurity regions 105 are formed by implanting phosphorous ions at an acceleration energy of 10-30 keV (Iwata at col. 11, lines 1-15). Thereafter, the impurities are activated at 850 to 900 °C (Iwata at col. 11, lines 59-64). Thereafter, third impurity regions 108 are formed by implanting arsenic ions at 20-40 keV (Iwata at col. 12, lines 34-40).

However, Applicant respectfully submits that Iwata clearly does not teach or suggest a method of forming a semiconductor device in which arsenic is implanted at a first acceleration energy (e.g., to form source/drain regions) *"wherein said first acceleration energy is no greater than 15keV"* , as recited, for example, in claims 3 and 8.

As noted above, unlike conventional in which source/drain regions are formed by implanting arsenic at a high acceleration energy of about 50 keV in order to avoid a p-n junction leakage current, the claimed invention implants arsenic at an acceleration energy

which is no greater than 15keV (e.g., to form the source and drain regions). The inventors found that implanting phosphorous into the arsenic implanted regions of the substrate helps to inhibit a leakage current. Thus, the claimed invention is able to implant arsenic at an acceleration energy (e.g., a low acceleration energy) which inhibits a reverse short channel effect without increasing the p-n junction leakage current (Application at page 14, lines 13-22).

The Application explains that the inventors of the claimed invention found that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse shallower than phosphorous ions implanted without a previous arsenic implantation (Application at page 11, lines 1-5). This is because the point defects generated by the phosphorous ion implantation are absorbed by the amorphous silicon layer generated by the arsenic ion implantation, so that the diffusion of the phosphorous ion assisted by the point defects is weakened (Application at page 11, lines 6-10).

Therefore, the inventors have discovered that by implanting phosphorous after implanting arsenic, the distance between the amorphous silicon/ monocrystalline silicon interface and a p-n junction interface can be increased. This allows the arsenic implantation energy to be reduced to eliminate the reverse short channel effect, without causing the p-n junction leakage current to increase (Application at page 10, lines 15-22).

Clearly, Iwata does not teach or suggest these novel features. Indeed, as noted above, Iwata does not even recognize one of the discoveries made by the inventors of the claimed invention, namely that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse shallower than phosphorous ions implanted without a previous arsenic implantation. As noted above, this allows the claimed method implant arsenic (e.g., to form source/drain regions) using an acceleration energy of about 15keV or less without causing a p-n junction leakage current.

Moreover, the Examiner concedes that Iwata does not teach or suggest implanting arsenic at an acceleration energy which is no greater than 15keV (e.g., to form the source and drain regions). However, he alleges that it would have been obvious to modify the Iwata method so as to implant the arsenic ions at this acceleration energy level. The Examiner is clearly incorrect.

In fact, the Application expressly states conventionally, the acceleration energy for the implantation of arsenic (e.g., to form source/drain regions) was 50 keV. Although it was known that the acceleration energy level could be lowered to reduce the reverse short channel effect, this was not seriously considered since it was known to result in a p-n junction leakage current (Application at page 9, lines 5-19).

Indeed, only after the inventors discovered that implanting phosphorous after implanting arsenic may be used to reduce a p-n junction leakage current, was it known that the acceleration energy level of implanting arsenic could be lowered without experiencing the p-n junction leakage current. Clearly, this understanding is not taught or suggested in Iwata Therefore, contrary to the Examiner's allegations no person of ordinary skill in the art at the time of filing the Application would have considered reducing the acceleration energy level for implanting arsenic (e.g., to form source/drain regions) from 50 keV.

Therefore, it is clearly unreasonable to suggest that one of ordinary skill in the art would have modified the process of Iwata to form the claimed invention.

Therefore, Applicant submits that Iwata does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

Applicant notes that claim 14 has been amended to address the Examiner's objection thereto.

This Amendment includes an amendment to the specification. Applicant notes that the sentence added by this Amendment was recited in claim 6 of the present Application as originally filed.

In view of the foregoing, Applicant submits that claims 3-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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